Gate current degradation in W-band InAlN/AlN/GaN HEMTs under Gate Stress

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Purpose

To understand degradation of gate leakage current

in ultra-scaled InAlN/AlN/GaN HEMTs

under positive gate stress

Outline

1. Motivation
2. Devices and experimental approach
3. Gate stress experiments
   - Harsh step-stress (-recovery) experiments
   - Mild constant gate stress experiment
4. Thermal stress
5. Gate current: dominant charge transport mechanisms
6. Conclusions

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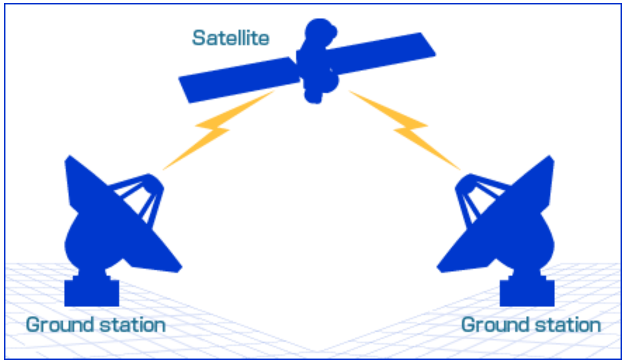
Benefits of GaN for RF

Promising applications:



Benefits of GaN for RF:

- Wide bandwidth
- High power density
- Excellent energy efficiency
- Small volume

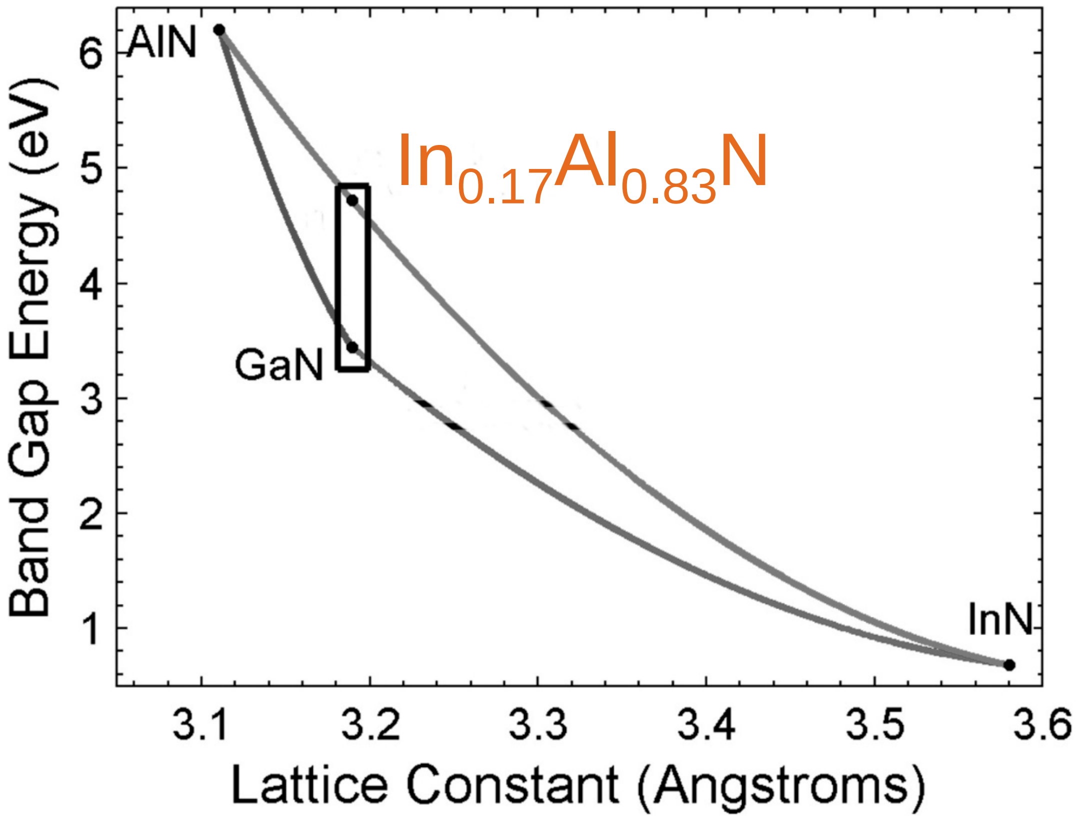
InAlN as barrier material

	$Al_{0.2}Ga_{0.8}N/GaN$	$In_{0.17}Al_{0.83}N/GaN$
ΔP_0 (cm^{-2})	6.5×10^{12}	2.7×10^{13}
P_{piezo} (cm^{-2})	5.3×10^{12}	0
P_{total} (cm^{-2})	1.2×10^{13}	2.7×10^{13}

[J. Kuzmik, EDL 2001]

- High spontaneous polarization in InAlN → high 2DEG density
- InAlN thickness scaling → gate length scaling
  → W- and V-band applications

InAlN as barrier material



[M. A. Laurent, JAP 2014]

$In_{0.17}Al_{0.83}N$ lattice matched to GaN

→ Potentially better reliability!

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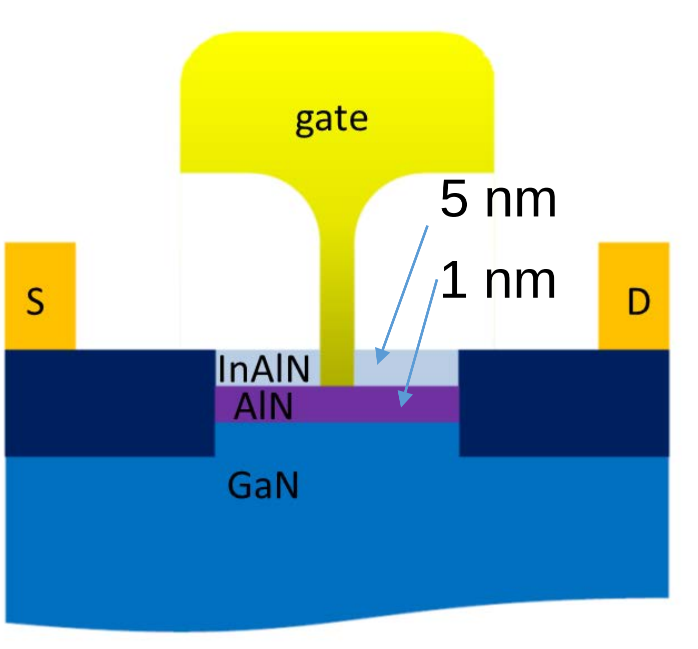
Devices (E-mode)

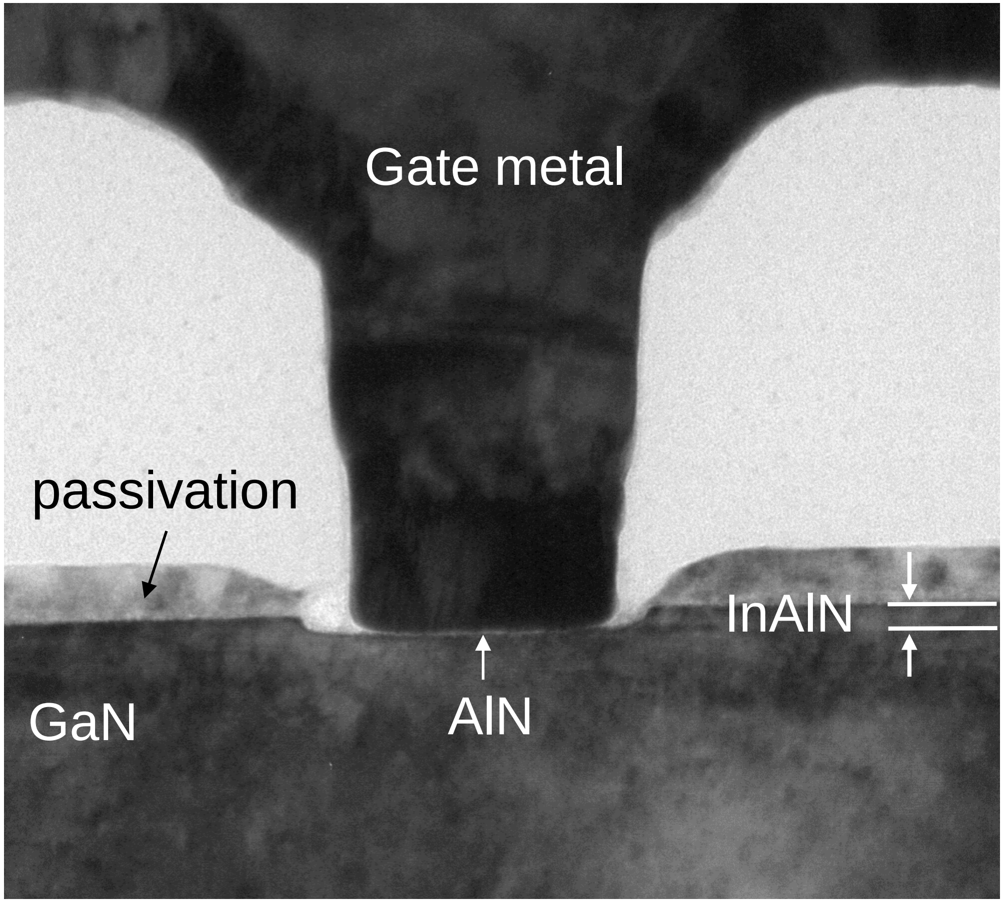
InAlN/AlN/GaN HEMTs:

- E-mode
- L_g = 40 nm
- L_{gs}=L_{gd}=1 µm
- W-band



[Saunier, CSICS 2014]

BFTEM of virgin device

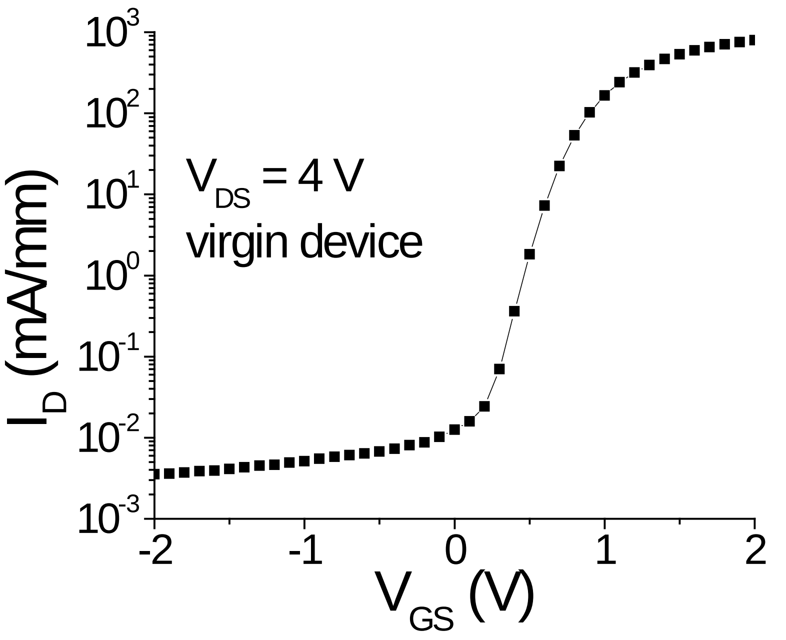


Thermal models available

FOMs for benign characterization, detrapping methodology

FOMs:

- I_{Dmax} : I_D at V_{GS} = 2 V and V_{DS} = 4 V
- V_{Tsat} : V_{GS} extrapolated from I_D at peak g_m point at V_{DS} = 4 V
- I_{Goff} : I_G at V_{GS} = -2 V, V_{DS} = 0.1 V
- I_{Doff} : I_D at V_{GS} = -2 V, V_{DS} = 0.1 V
- R_D : at I_G = 20 mA/mm
- R_S : at I_G = 20 mA/mm



Detrapping & initialization:

- 100 °C bake for 1 hour

Impact of characterization and detrapping

Impact of 200 successive characterizations

	$\Delta I_{Dmax}/I_{Dmax}(0)$ [%]	ΔV_{Tlin} [mV]	$R_D/R_D(0)$	$R_S/R_S(0)$
After initialization	0	0	1	1
After 200 characterizations	0.70	-23.4	0.95	0.89
After detrapping	0	2.3	1.01	1

Nearly complete recovery after thermal detrapping step
→ characterization suite is benign and detrapping step is effective

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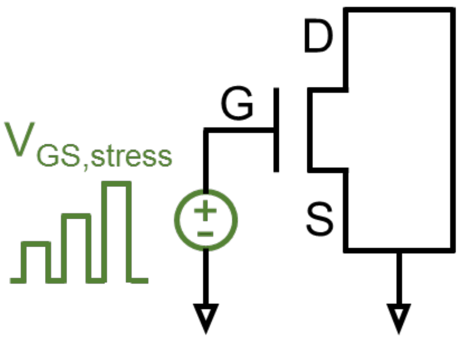
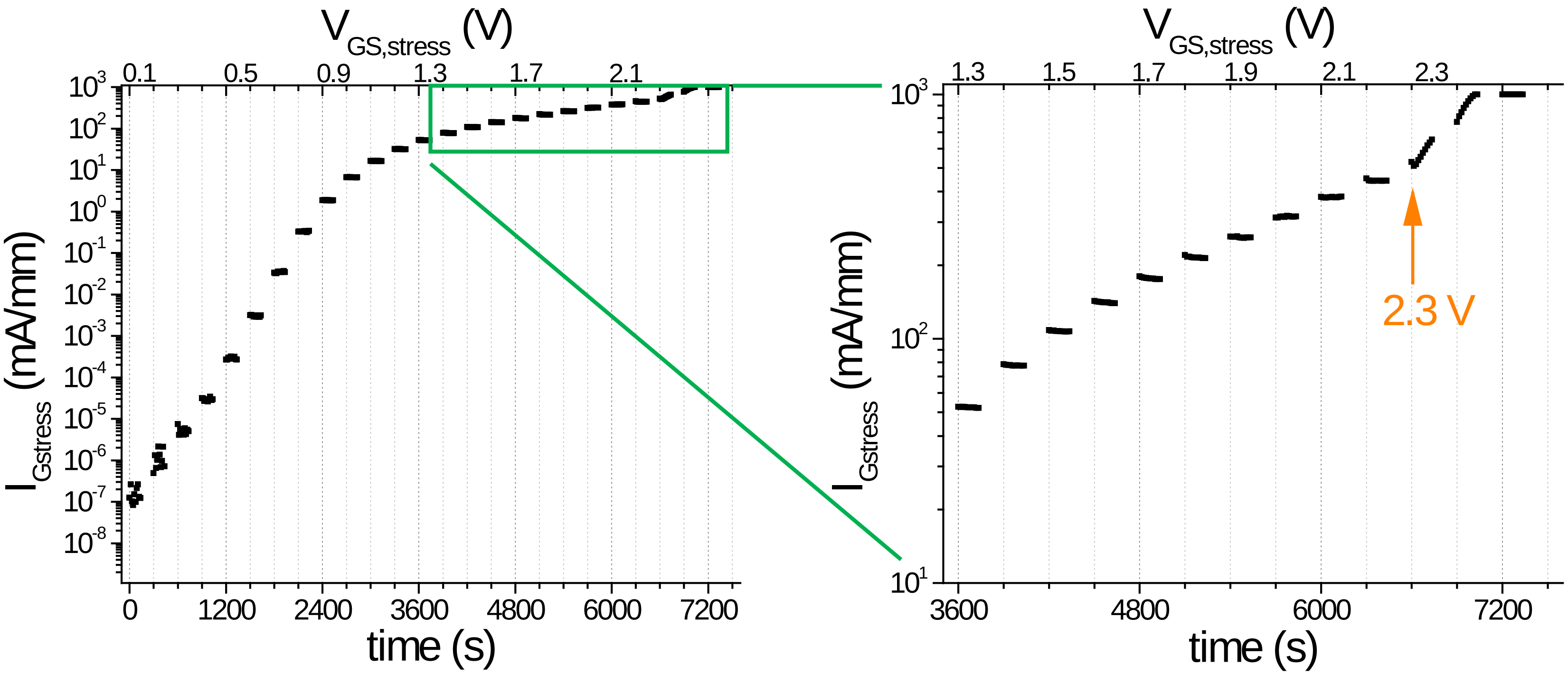
RT Positive-V_G step-stress-recovery experiment

Stress conditions:

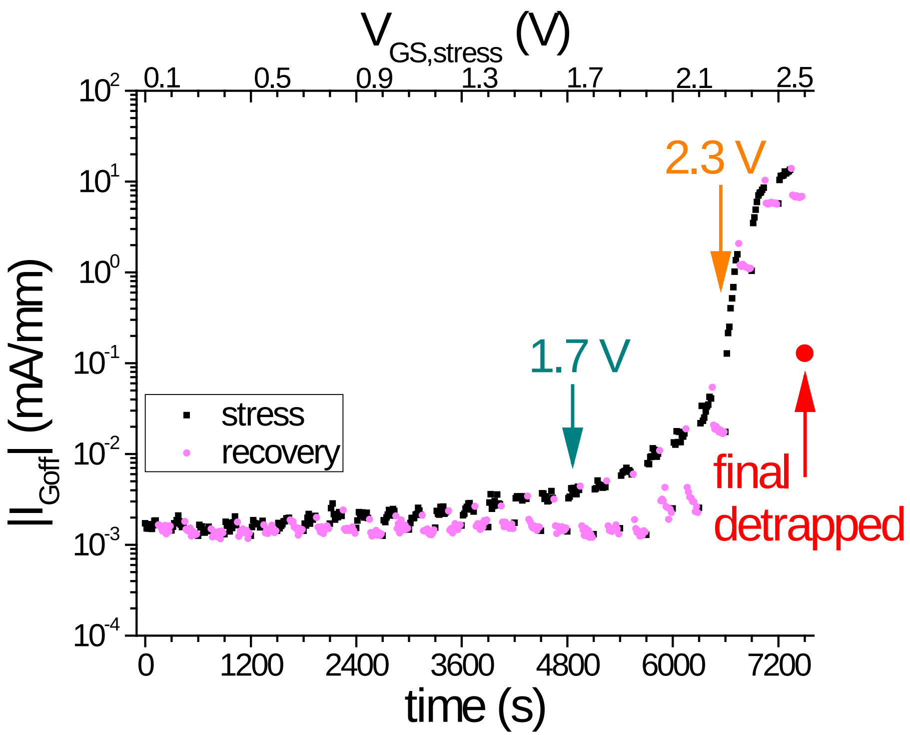
- $V_{GS,stress}$ = 0.1 – 2.5 V in 0.1 V steps, V_{DS} = 0 V, RT
- Recovery: V_{DS} = V_{GS} = 0 V
- Stress time = recovery time = 150 s
- Characterization every 15 s

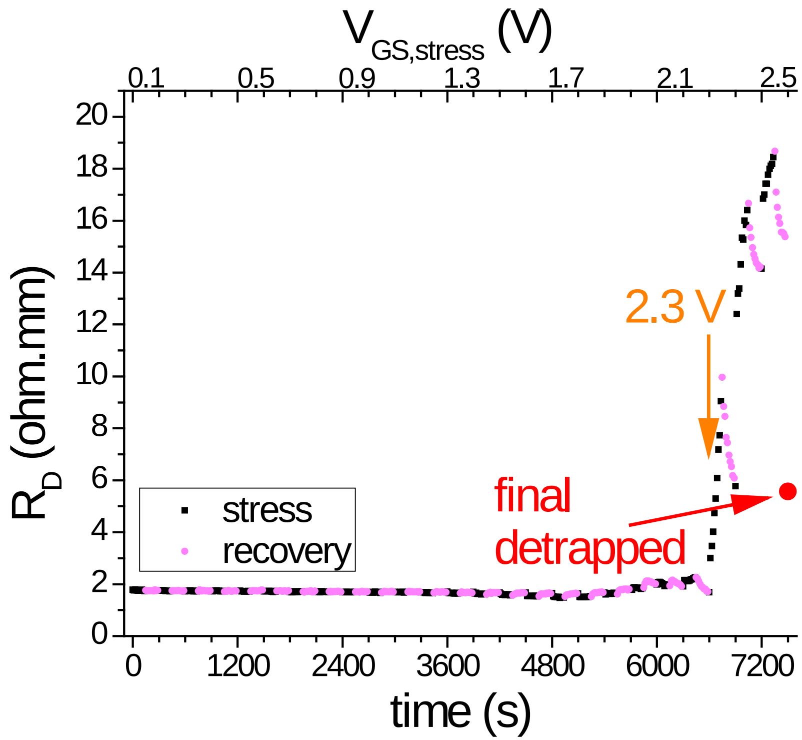




- $I_{Gstress}$ ↑ at constant $V_{GS,stress}$ for $V_{GS,stress}$ ≥ 2.3 V

Time evolution of I_{Goff} and R_D



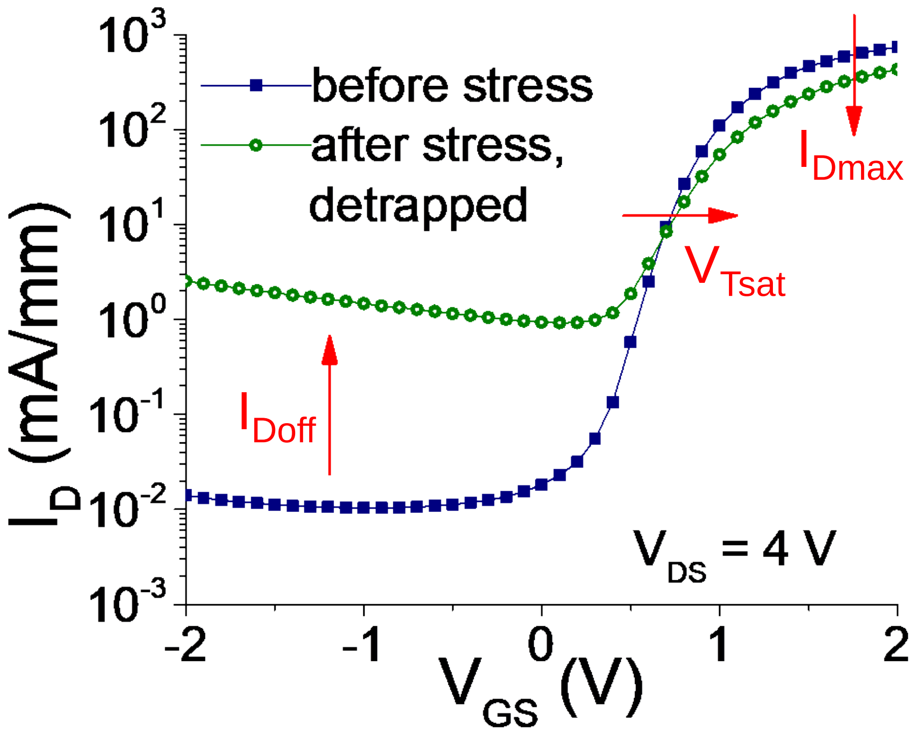


Two mechanisms:

- From $V_{GS,stress}$ = 1.7 V: I_{Goff} ↑, trapping ↑ → mechanism 1: new defects generated in AlN
- From $V_{GS,stress}$ = 2.3 V:
  - o I_{Goff} ↑↑
  - o R_D and R_S ↑↑

} Mechanisms 2 ?

Before and after stress: permanent degradation



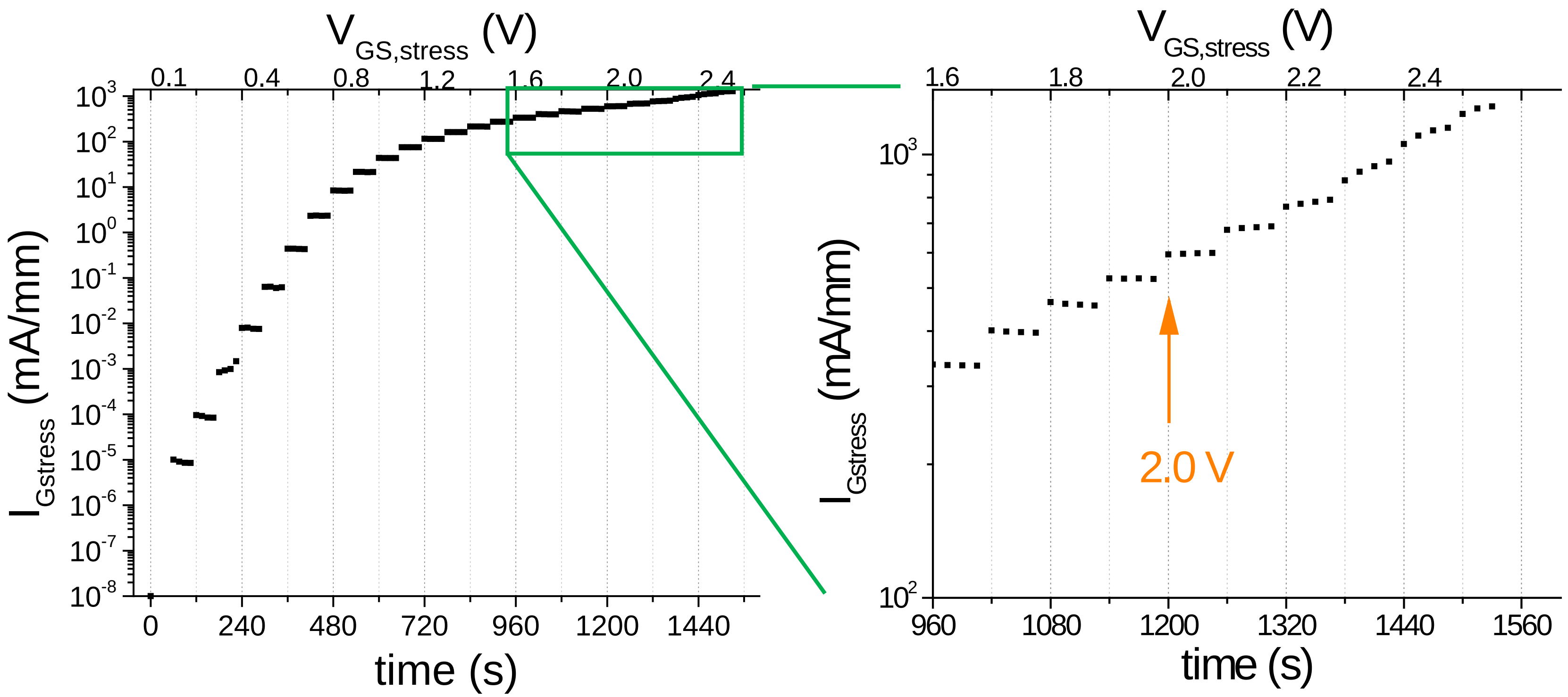
- I_{Doff} ↑↑
- I_{Dmax} ↓
- $\Delta V_{Tsat} > 0$

} Mechanisms 2: consistent with gate sinking

High T Positive-V_G step-stress experiment

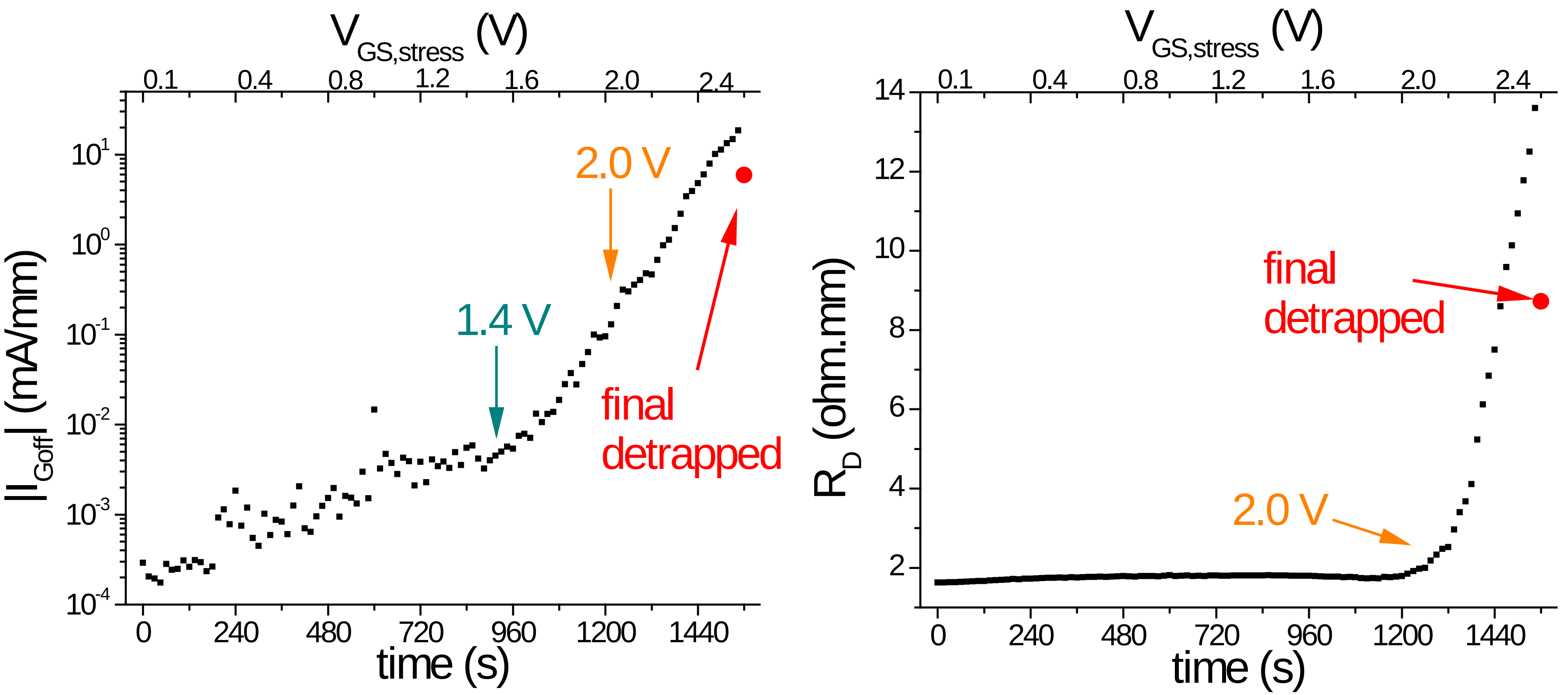
Stress conditions:

- $V_{GS,stress}$ = 0.1 – 2.5 V in 0.1 V steps, V_{DS} = 0 V, T_{stress} = 150 °C
- Stress time = 60 s
- Characterization every 15 s



- $I_{Gstress}$ ↑ at constant $V_{GS,stress}$ for $V_{GS,stress}$ ≥ 2.0 V

High T Positive-V_G step-stress experiment



- From $V_{GS,stress}$ = 1.4 V: I_{Goff} ↑
- From $V_{GS,stress}$ = 2.0 V: I_{Goff}, R_D, and R_S ↑↑
- Lower threshold for degradation than at RT → Both mechanisms thermally enhanced

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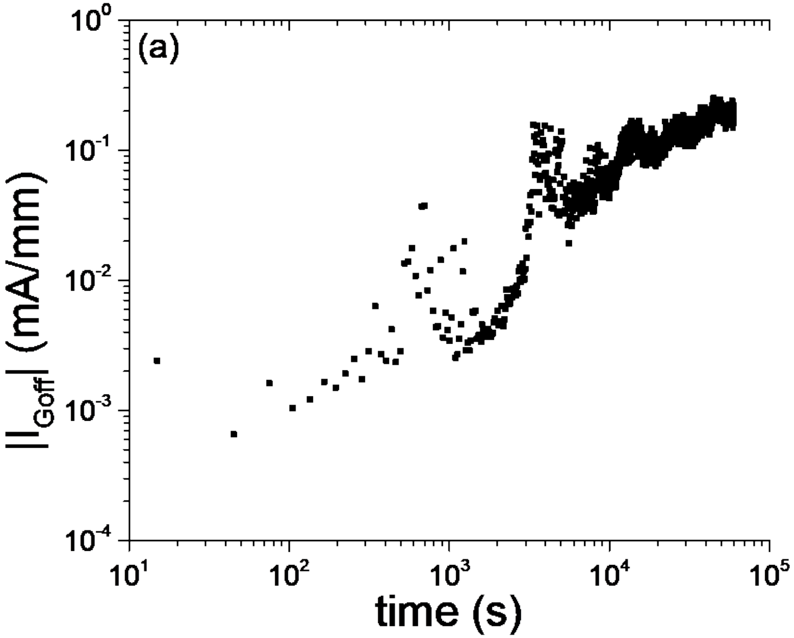
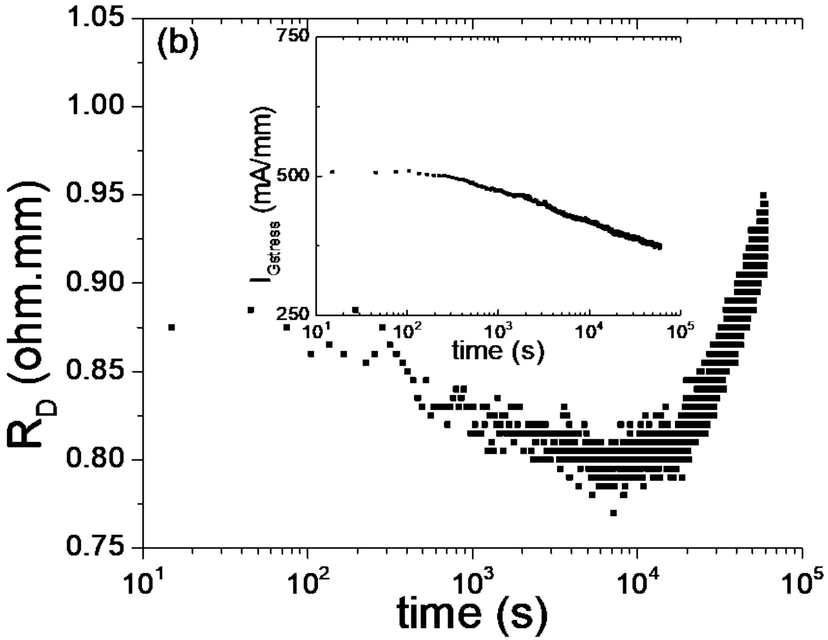
RT Constant-V_G stress experiment

Stress conditions:

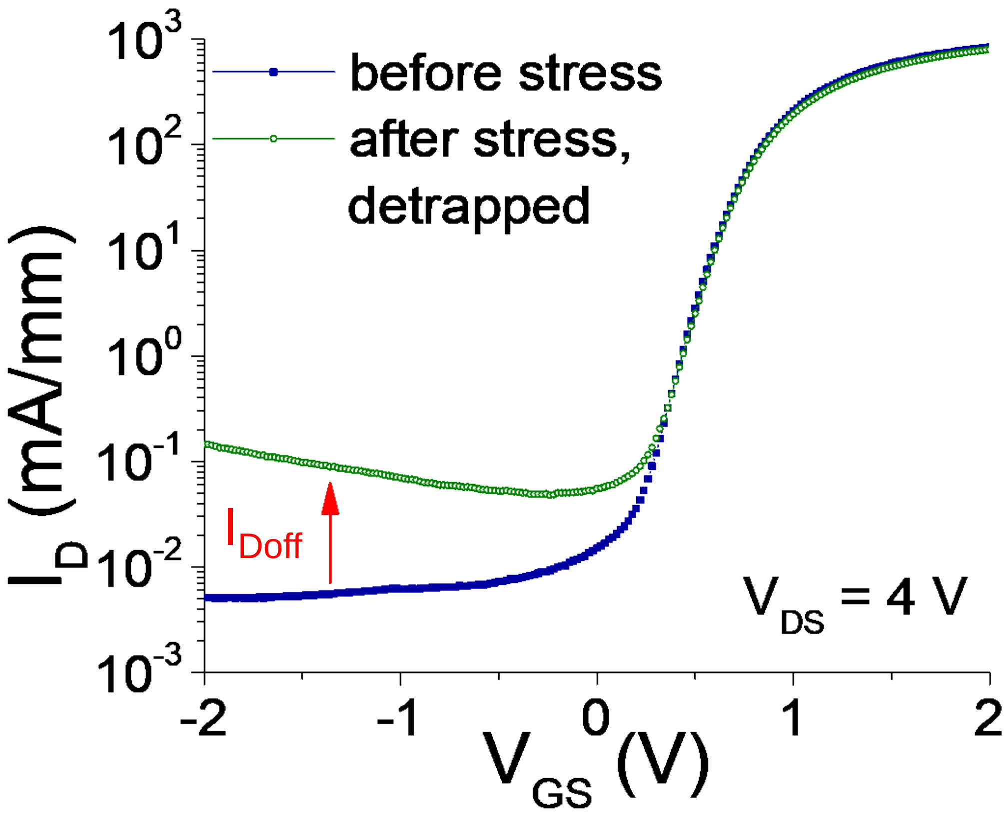
- $V_{GS,stress}$ = 2 V, V_{DS} = 0 V, RT
- Characterization every 15 s





- I_{Goff} becomes noisy at t_{stress} ~ 500 s; increases afterwards → consistent with trap generation in AlN layer (mechanism 1)
- R_D changes little throughout experiment
- $I_{Gstress}$ keeps decreasing → no Schottky barrier degradation

Before and after stress: permanent degradation



- I_{Doff} ↑↑
- No significant I_{Dmax} degradation
- No significant subthreshold characteristics degradation

Summary so far

Two degradation mechanisms identified:

1. Under mild gate stress:
   - Observation: I_{Goff} ↑, trapping ↑, thermally enhanced
   - Proposed mechanism 1: high electric field induced defect generation in AlN interlayer
2. Under harsh gate stress:
   - Observation: I_{Goff} ↑, R_D and R_S ↑, $\Delta V_T > 0$, I_{Dmax} ↓, thermally enhance
   - Proposed mechanism 2: self-heating induced Schottky gate degradation, or gate-sinking

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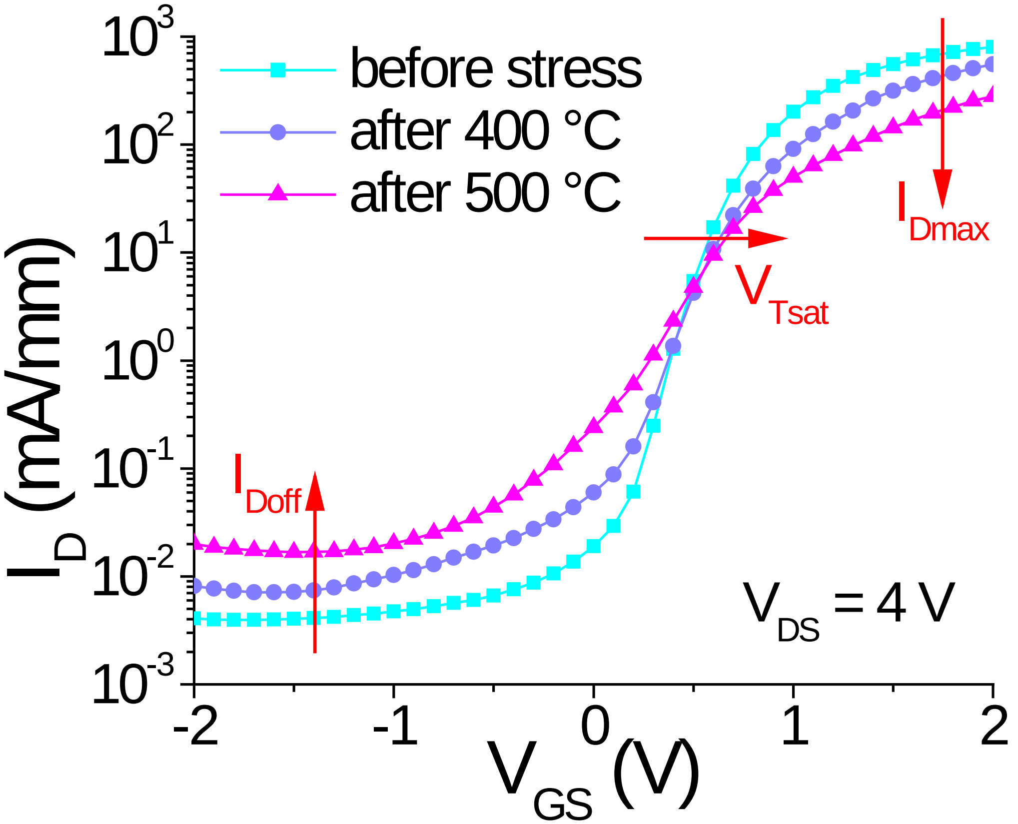
Thermal stress experiment

Impact of thermal stress: 1 min. RTA in N_2



Permanent degradation:

- Prominent I_{Dmax} ↓ with T
- Positive V_{Tsat} shift
- I_{Doff} ↑

Same signature as that of degradation mechanism 2
→ consistent with gate sinking

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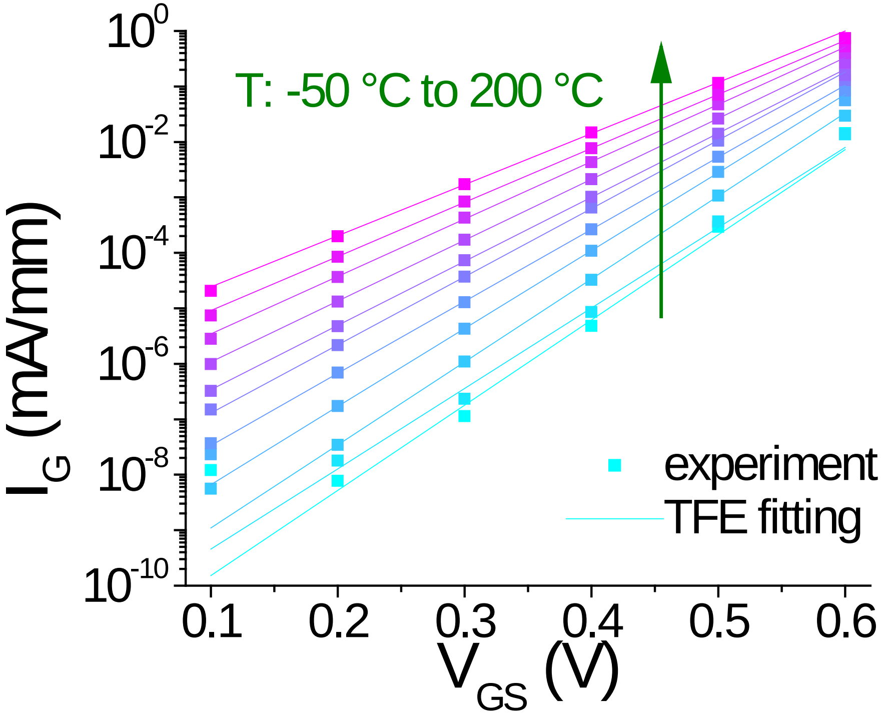
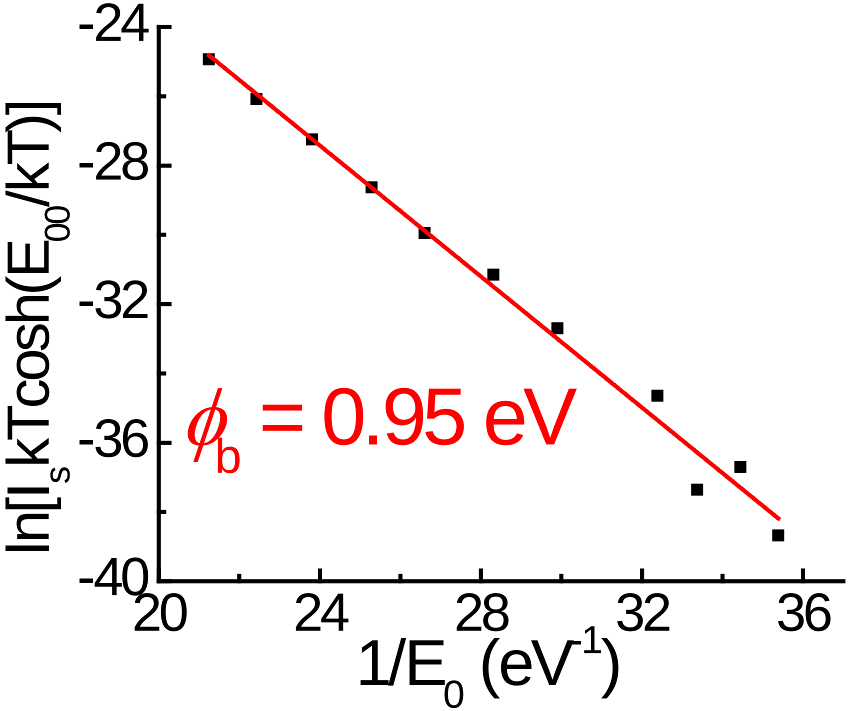
Virgin device: Thermionic Field Emission fitting

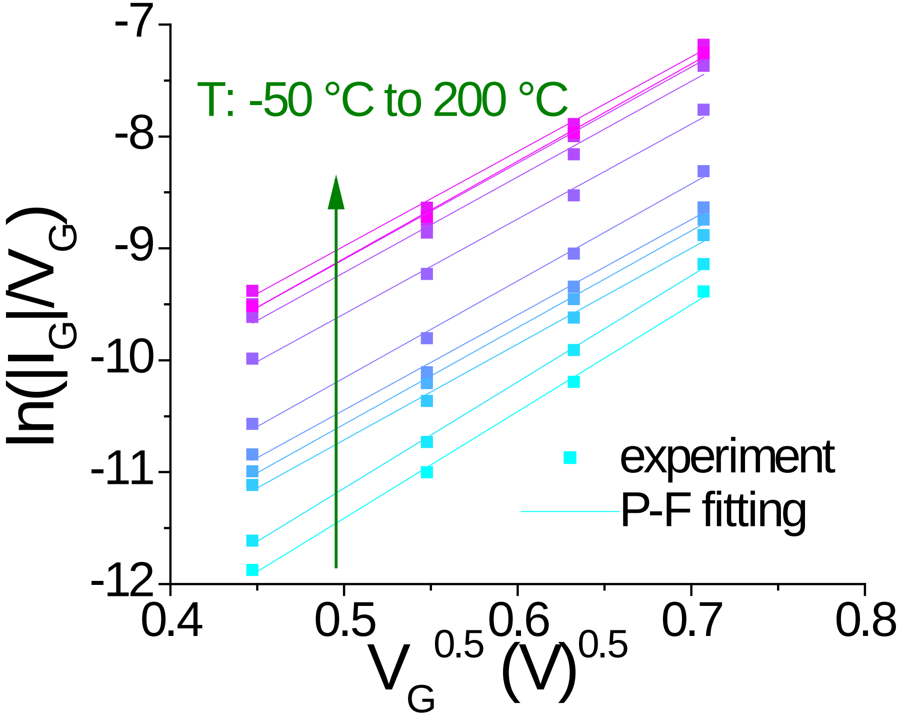


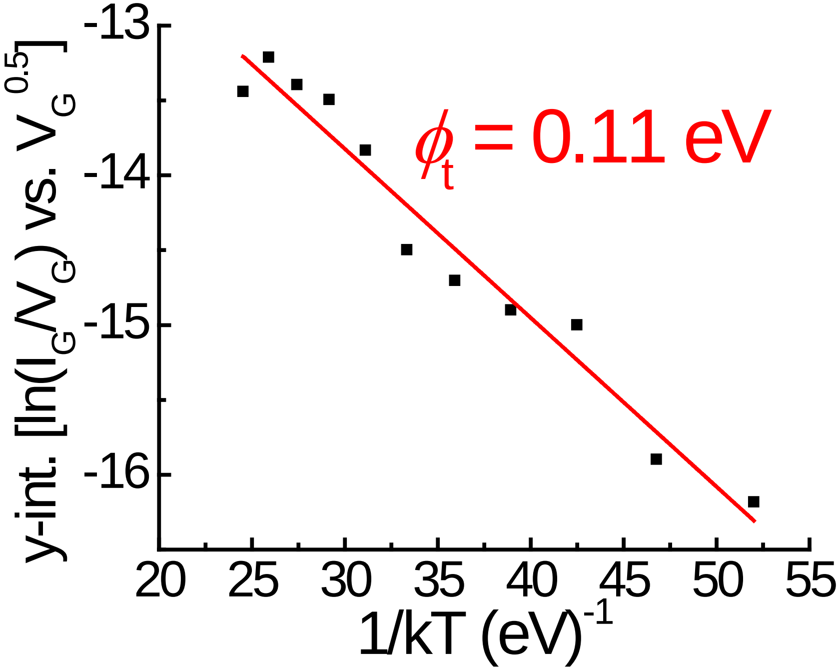


- T dependence well explained by Thermionic Field Emission (TFE) theory
- Extracted effective Schottky barrier height (ϕ_b): 0.95 eV

After harsh gate stress: Poole-Frenkel Emission fitting

Stress conditions: $V_{GS,stress}$ = 0 – 2.5 V in 0.1 V steps, V_{DS} = 0 V

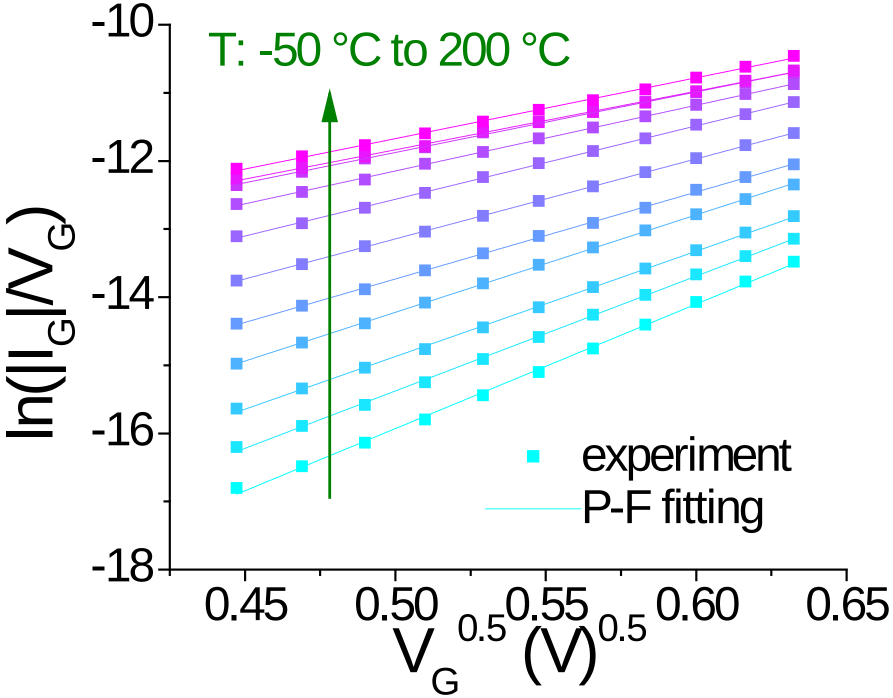


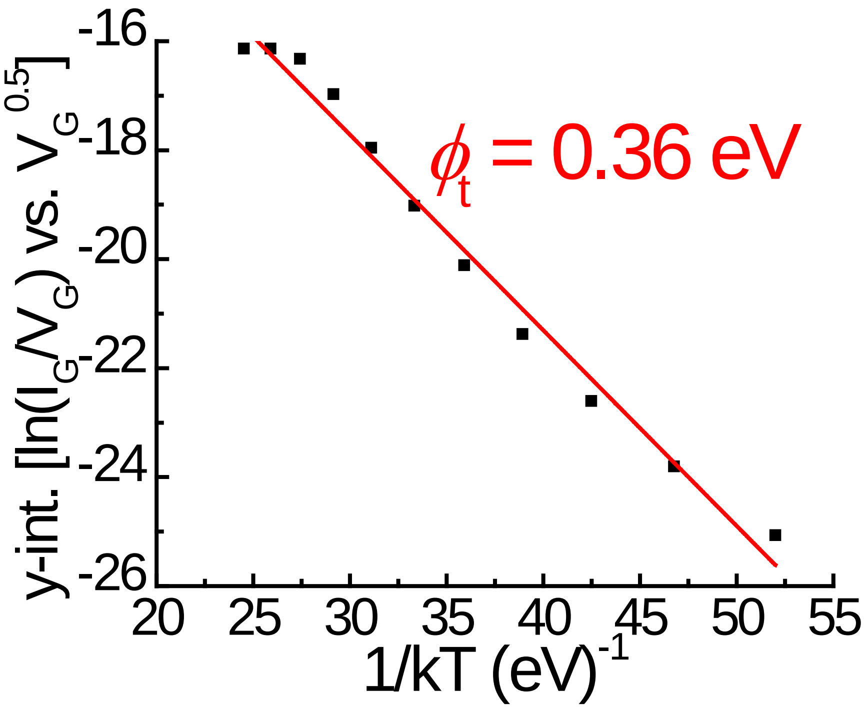


- T dependence well explained by Poole-Frenkel Emission (P-F) theory
- Extracted effective trap energy level (ϕ_t): 0.11 eV

After mild gate stress: Poole-Frenkel Emission fitting

Stress conditions: $V_{GS,stress}$ = 2 V, V_{DS} = 0 V





- T dependence well explained by Poole-Frenkel Emission (P-F) theory
- Extracted effective trap energy level (ϕ_t): 0.36 eV
- Close to donor level of N vacancy in AlN of 0.5 eV [T. L. Tansley, PRB 1992]

Outline

Conclusions

Identified two degradation mechanisms:

1. Under mild gate stress:
   - Observation: I_{Goff} ↑, trapping ↑, thermally enhanced
   - Proposed mechanism 1: high electric field induced defect generation in AlN interlayer
2. Under harsh gate stress:
   - Observation: I_{Goff} ↑, R_D and R_S ↑, $\Delta V_T > 0$, I_{Dmax} ↓, thermally enhanced
   - Proposed mechanism 2: self-heating induced Schottky gate degradation, or gate-sinking

Transport model for I_G in low forward regime:

- Virgin device: TFE with ϕ_b = 0.95 eV
- After degradation mechanism 1: P-F with ϕ_t = 0.36 eV
- After degradation mechanism 2: P-F with ϕ_t = 0.11 eV